**Lab 1**

**How to Use Xilinx ISE 12.1 Project Navigator**

**Acknowledgements:** Developed by Bassam Matar, Engineering Faculty at Chandler-Gilbert Community College, Chandler, Arizona. *Funded by National Science Foundation (NSF).*

Lab Summary:

This is a voluntary lab, for those of you who lack experience in the use of Xilinx ISE 12.1©. We will walk you through a small version of a lab session and produce a totally fake lab report. In the process, though, you will use all of the main steps that you will be asked to use in all later lab work.

This lab will present design entry, simulation, and prototyping with tools that are provided by Xilinx® ISE 12.1 for this purpose. We will show how a simple design circuit of 2 inputs AND gate can be directly entered into Xilinx® ISE 12.1 for synthesis, post synthesis simulation and timing analysis. We will show the implementation of more complex designs in future labs by running them through the design flow illustrated in this lab.

**Lab Goal:** The goal of this lab is to learn the use of using Xilinx® ISE 12.1 software by implementing inputs and outputs for a simple 2 inputs AND gate.

**Learning Objectives**

1. Create a 2 input AND gate project in Xilinx® ISE 12.1 using the free software **ISE** WebPACK.
2. Use the Xilinx® ISE 12.1 Schematic Editor to enter a graphical design in Xilinx® ISE 12.1
3. Compile and simulate the 2 inputs-AND design.
4. Compile and simulate the 4 inputs -XOR design.

**Grading Criteria:** Your grade will be determined by your instructor.

**Time Required**: 2-3 hours

**Lab Preparation**

* Read this document completely before you start on this experiment.
* Print out the laboratory experiment procedure that follows.

**Equipment and Materials**

Access to Xilinx software

|  |  |
| --- | --- |
| **Software needed** | **Quantity** |
| The following items from the Xilinx: www.xilinx.com   * free software **ISE** WebPACK | 1 |

Additional References:

* Xilinx ISE 12.1 Software manuals found on Xilinx web site: www.xilinx.com

**Simulation Lab 1**

In this lab, you will first load and license the Xilinx® ISE 12.1 using the free software **ISE** WebPACK. Then you will be given some small circuit of limited functionality.

Installing Xilinx ISE 12.1 Software

**Step 1:**

**Register with Xilinx at** [www.xilinx.com](http://www.xilinx.com)**. Download ISE Webpack. Select download from the top menu, then on the right hand side, select** ISE WebPACK™ to download.

**Step 2:**

**Install ISE Webpack.**

***There might be newer version of ISE since I wrote this lab. However, there should not be a lot of changes in the instruction between 12.1i version and the newer one. I recommend that you download the 12.1 version.***

### System Requirements

* Microsoft Windows XP Professional,7, Vista or Linux.

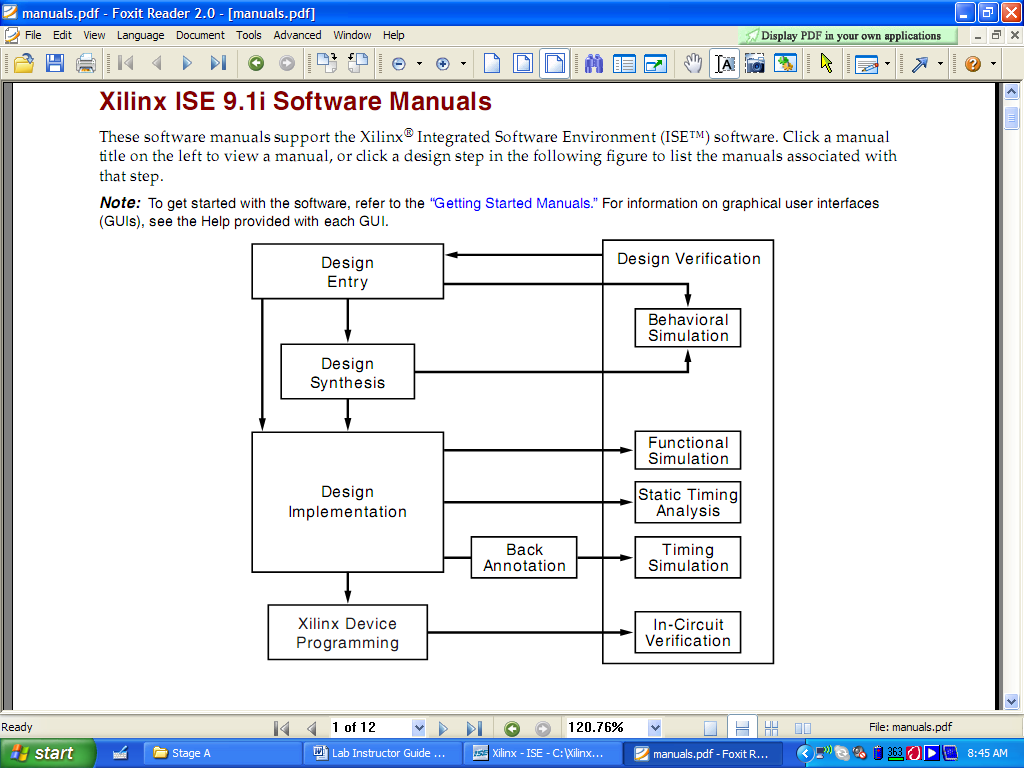
**Step 3:**

**Have Fun!**

**Lab Procedure: Building AND-2 Circuit**

**Xilinx Design process:**

**Step 1: Design Entry**



* Two design methods: HDL (Verilog or VHDL) or schematic drawings.

*For the simulation part of our class, we will use schematic method and VHDL.*

**Step 2: Design Synthesis**

* Translate VHDL and schematic files into an industry standard format EDIF file.

**Step 3: Design Implementation**

* Translate Map, Place and Route. This process will generate a configuration file (.JED) for FPGA programming**.**

**Step 4: Xilinx Device Programming**

* Download JED file into FPGA

In this portion of the lab, you will use Xilinx ISE 12.1 Software to build AND-2 circuit. The steps involved are design entry and synthesis. We will implement Steps 3 and 4 in our hardware labs.

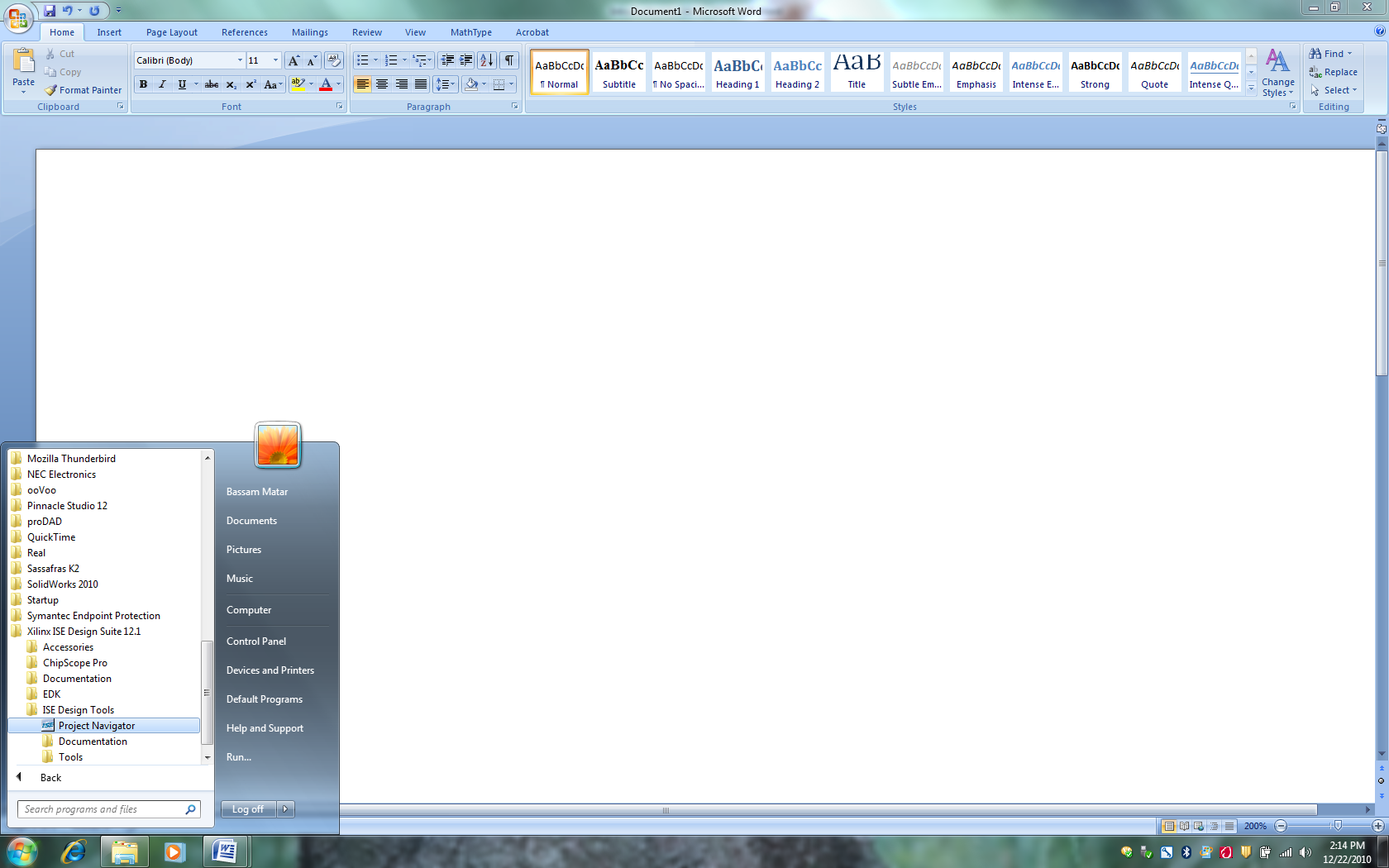
NOTE: At the conclusion of the lab, you will be asked to comment on why certain steps are required. Be sure to take notes on these questions as they appear in the lab procedure.

**Step 1: Design Entry**

**Design Entry Instructions**

1. Open Xilinx ISE 12.1 edition software

a. Select Start



b. All Programs

c. Xilinx ISE Design Suite 12.1

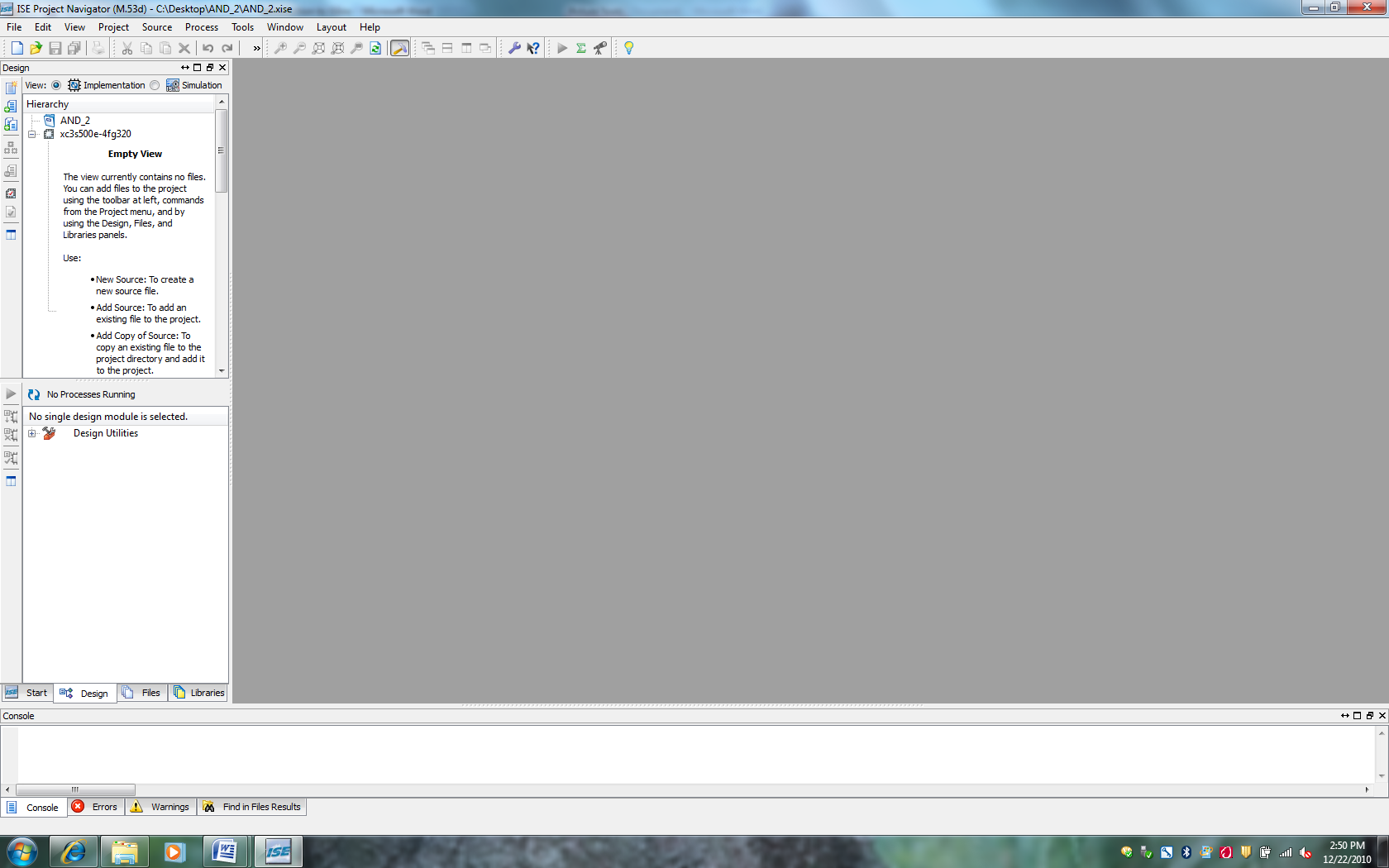
d. ISE Design Tools

d. Project Navigator

|  |  |
| --- | --- |
| 1. The starting windows should look like this |  |

|  |  |
| --- | --- |
| 2. Create a new project by selecting: **File** from the main menu **New Project**   1. In the New Project window, name your project *AND\_2* in the project name text box. 2. In the **Project Location** selection box, enter the folder or directory where your project will be saved. Use your name for *Desktop* and locate the place where you want to save all your files (i.e C:\) 3. Under **Top-Level Source Type**, select **HDL** and 4. click **Next**. | Pic4 |
| 3. We will design our AND-2 for a particular device “Spartan 3E FPGA”.  **Product Category:** General Purpose  **Family:** Choose **Spartan 3E**, the device we will be using.  **Device**: **XC3S500E**, the specific Spartan 3E device we use. This is actually printed (very small) on the FPGA package which you will see in the hardware lab.  **Package:** FG320, this is the package type of our device (Ball Grid Array, 320 pins)  **Speed Grade**: The speed grade for this device is -5.  **Preferred Language**: VHDL |  |

Hit the ***Next*** button and then click ***Finish*** to complete the process and verify the file name and type.



|  |  |
| --- | --- |
| 1. Now, you need to add a new source “Schematic” to your project. Add schematic by selecting **Project🡪New source.** Type, AND-2 as shown and click ***Next*** and then ***Finish***. Make sure you select “**Schematic**”   Please note AND-2 is just a name for your schematic. You can name the schematic file any name you desire. |  |
| 1. The window schematic is shown below. The file name of “AND-2” appears on the top left under **Sources** section. |  |
| 1. In order to select the 2-input AND gate, you need to select **Symbols** tab as shown below. |  |

|  |  |
| --- | --- |
| 1. Now the screen should look like this. Select AND2 and place it on the schematic editor screen as shown. |  |
| 1. Use the Zoom-in and Zoom out buttons to get a view similar to below figure. | Pic13 |

|  |  |
| --- | --- |
| 1. Next, we need to add wires to connect the pins and gates of our schematic. Select “Add Wires” from the shortcut menu:   Extend wire from both the inputs and outputs of the AND gate. |  |

**Accessing Help**

At any time during the tutorial, you can access online help for additional information about the ISE software and related tools.

|  |  |
| --- | --- |
| To open Help, do either of the following:   * Press **F1** to view Help for the   specific tool or function that you have  selected or highlighted.   * Launch the **ISE Help Contents**   from the Help menu. It contains  information about creating and maintaining  your complete design flow in ISE. | *Pic14* |

**Adding an I/O Marker**

An I/O marker is an input, output, or bidirectional signal. This establishes net polarity (direction of signal flow) and shows that the net is externally accessible. Without pins, the device is meaningless. All primary inputs and outputs must be marked with I/O markers as follows.

a) Select Add > I/O Marker, or click the Add I/O Marker toolbar button tools-iomarker.

b) In the [**Add I/O Markers Options**](file:///C:\Xilinx91i\doc\usenglish\help\iseguide\mergedProjects\ecs\html\ecs_hidd_dgiomarkeroptionspage.htm) that appear in the [**Options tab**](file:///C:\Xilinx91i\doc\usenglish\help\iseguide\mergedProjects\ecs\html\ecs_hid_tooloptiondlg.htm), select one of the following options to control the polarity of the marker:

For input, select:

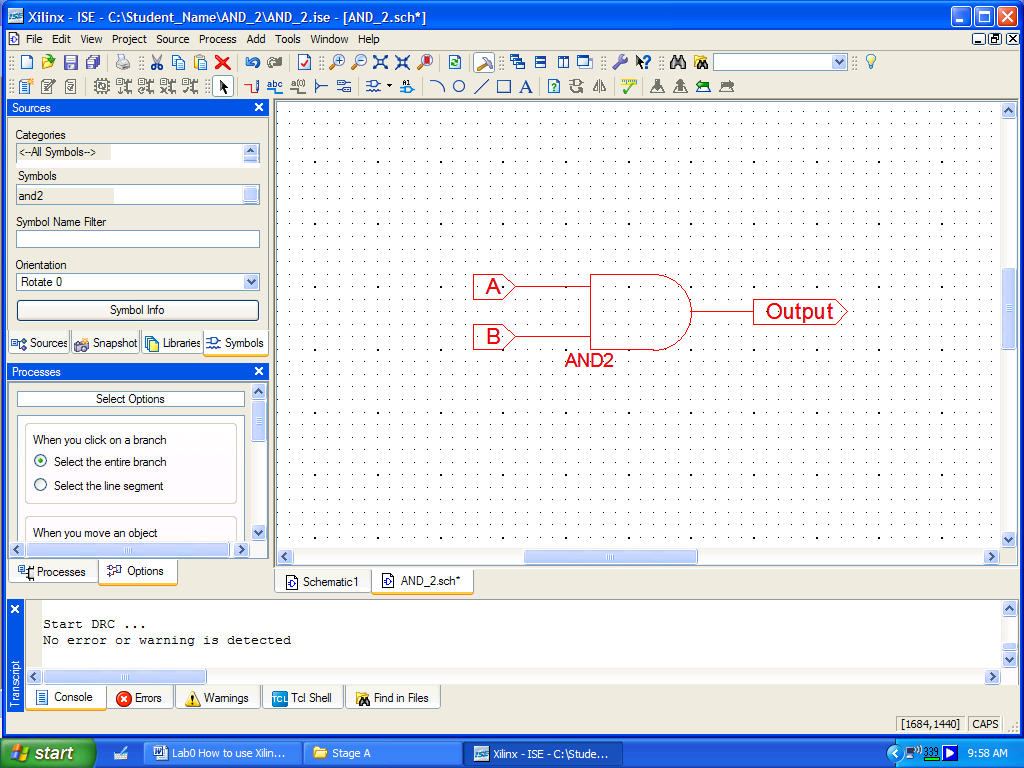
* Add an input marker

For output, select:

* Add an output marker

Attach input pins **A** and **B** to the schematic and outputs pin **OUT**.

|  |  |
| --- | --- |
| You can change the name of your input/output pins by simply clicking on the pin and hit the right mouse key to make the appropriate name change. | Pic16  Pic17 |



|  |  |
| --- | --- |
| Now our schematic is complete. To make sure your have the correct wiring, Check for errors. From **Tools**,  Select **Check Schematic.** | Pic18 |

In the status menu right under your schematic, you should get the message:

***Start DRC ...***

***No error or warning is detected***

***If not, review your steps and follow the lab procedures***

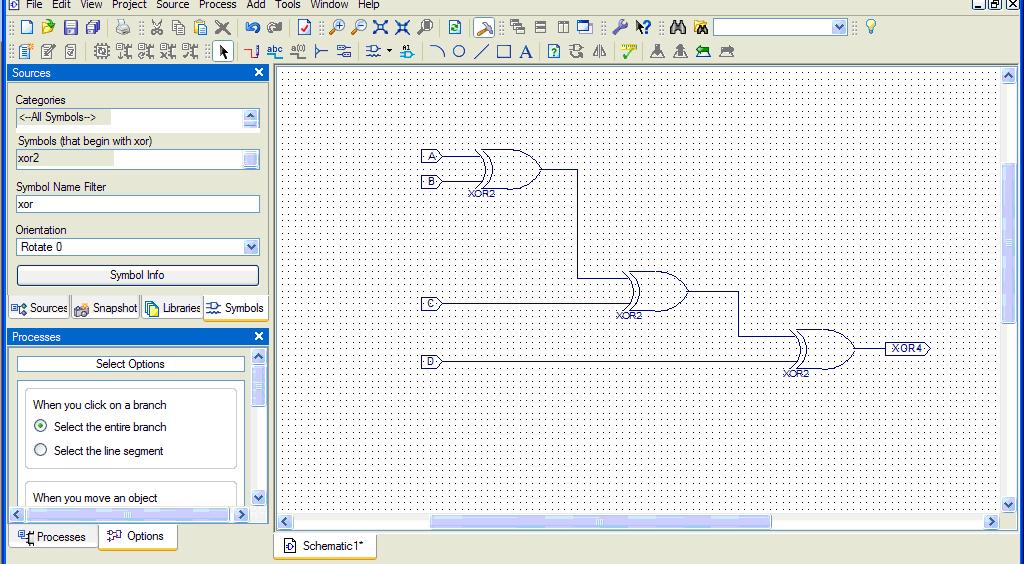
|  |  |
| --- | --- |
| Make sure you **save** your project by clicking on the save button off the shortcut menu. |  |

**Congratulation, you have successfully completed this practice lab.**

PRACTICE PRACTICE PRACTICE PRACTICE ………………..

The more you practice, the more you will be proficient with the software.

***Go to the next page for an exercise on what you have learned so far.***Build the following circuit (4 inputs XOR) using 2 inputs XOR gates.



|  |  |
| --- | --- |
| Now our schematic is complete. To make sure your have the correct wiring, Check for errors.  From **Tools**,  Select **Check Schematic.** | Pic18 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | B | C | D | **XOR4** |
| **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **1** | **0** | **1** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** | **1** |
| **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **0** |
| **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** | **1** |

***LIBRARY ieee;***

***USE ieee.std\_logic\_1164.ALL;***

***USE ieee.numeric\_std.ALL;***

***LIBRARY UNISIM;***

***USE UNISIM.Vcomponents.ALL;***

***ENTITY XOR\_CIRCUIT\_XOR\_CIRCUIT\_sch\_tb IS***

***END XOR\_CIRCUIT\_XOR\_CIRCUIT\_sch\_tb;***

***ARCHITECTURE behavioral OF XOR\_CIRCUIT\_XOR\_CIRCUIT\_sch\_tb IS***

***COMPONENT XOR\_CIRCUIT***

***PORT( D : IN STD\_LOGIC;***

***C : IN STD\_LOGIC;***

***B : IN STD\_LOGIC;***

***A : IN STD\_LOGIC;***

***XORGATE4 : OUT STD\_LOGIC);***

***END COMPONENT;***

***-- Initialize all inputs***

***SIGNAL D : STD\_LOGIC :='0';***

***SIGNAL C : STD\_LOGIC :='0';***

***SIGNAL B : STD\_LOGIC :='0';***

***SIGNAL A : STD\_LOGIC :='0';***

***-- output***

***SIGNAL XORGATE4 : STD\_LOGIC;***

***BEGIN***

***UUT: XOR\_CIRCUIT PORT MAP(***

***D => D,***

***C => C,***

***B => B,***

***A => A,***

***XORGATE4 => XORGATE4***

***);***

***-- \*\*\* Test Bench - User Defined Section \*\*\****

***tb : PROCESS (A,B,C,D)***

***SIGNAL A: PROCESS***

***BEGIN***

***A <= NOT A;***

***WAIT FOR 25 ns;***

***END PROCESS;***

***SIGNAL B: PROCESS***

***BEGIN***

***B <= NOT B;***

***WAIT FOR 50 ns;***

***END PROCESS;***

***SIGNAL C: PROCESS***

***BEGIN***

***C <= NOT C;***

***WAIT FOR 75 ns;***

***END PROCESS;***

***SIGNAL D: PROCESS***

***BEGIN***

***D <= NOT D;***

***WAIT FOR 100 ns;***

***END PROCESS;***